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are needed to see this picture.

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High Speed Optical Networking
Task 3: Progress Report

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Outline

- FEC Code Design: RCD Code - subset of LDPC Codes
- Channel Models for FEC Code and Decision Circuit
- Performance (Ideal) Assessment via Bounds and Simulation
- Performance (Non-Ideal) Assessment via Implementation Issues

FEC Code Design: RCD Codes

- Subset of Regular LDPC Codes
- Decodable via Variety of Decoder Schemes
  w/ Choice Driven by Performance vs. Technology Trade-offs
  - Majority-Logic (MLG) Decoding
  - Iterative Hard-Decision Decoding (Bit-Flipping)
  - Iterative Soft-Decision Decoding (SPA)
- High Code Rates (Low Overhead) Possible

LDPC vs. TC Codes

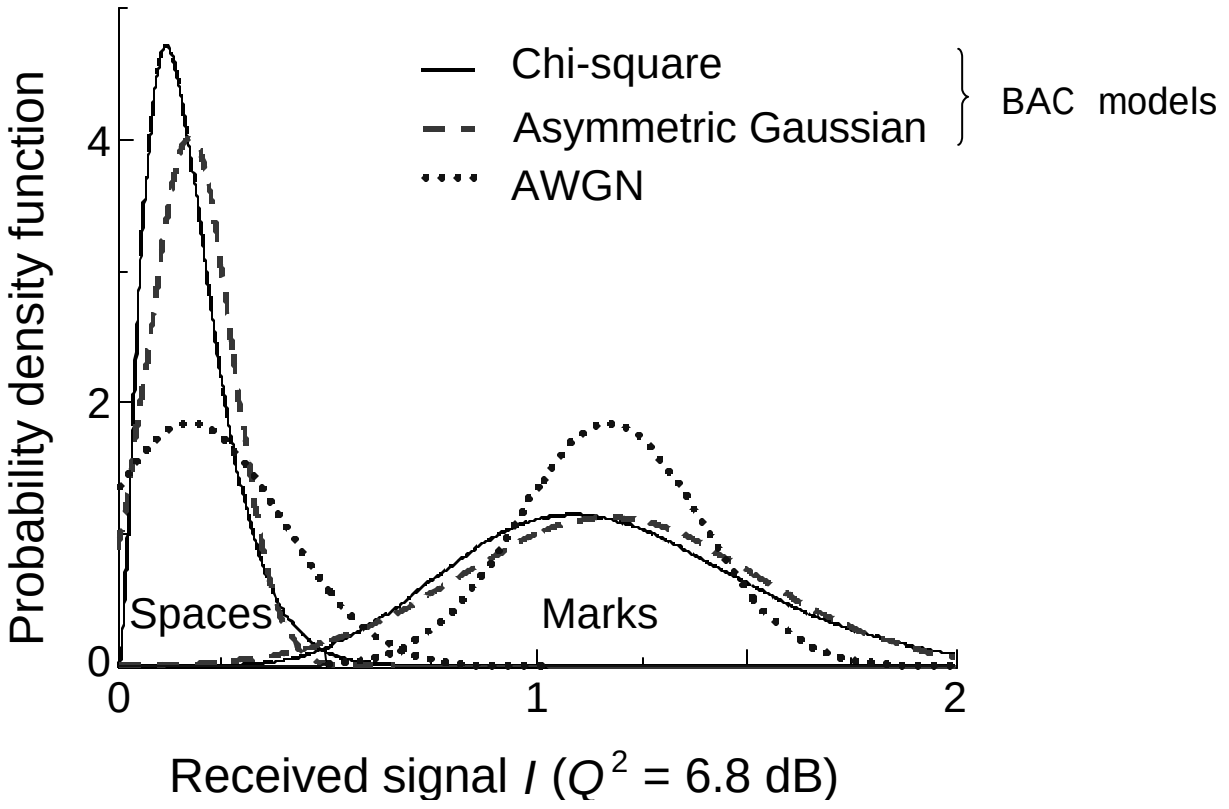
- Best designed LDPC codes shown to surpass corresponding best known turbo codes.
- For LDPC codes, decoder failure is a detectable event.
- TCCs show an error floor at a relatively higher probability of error. Hence, quite often, they require an outer code.
- LDPC decoding fully parallelizable with respect to graph nodes.

Channel Models for FEC Code and Decision Circuit

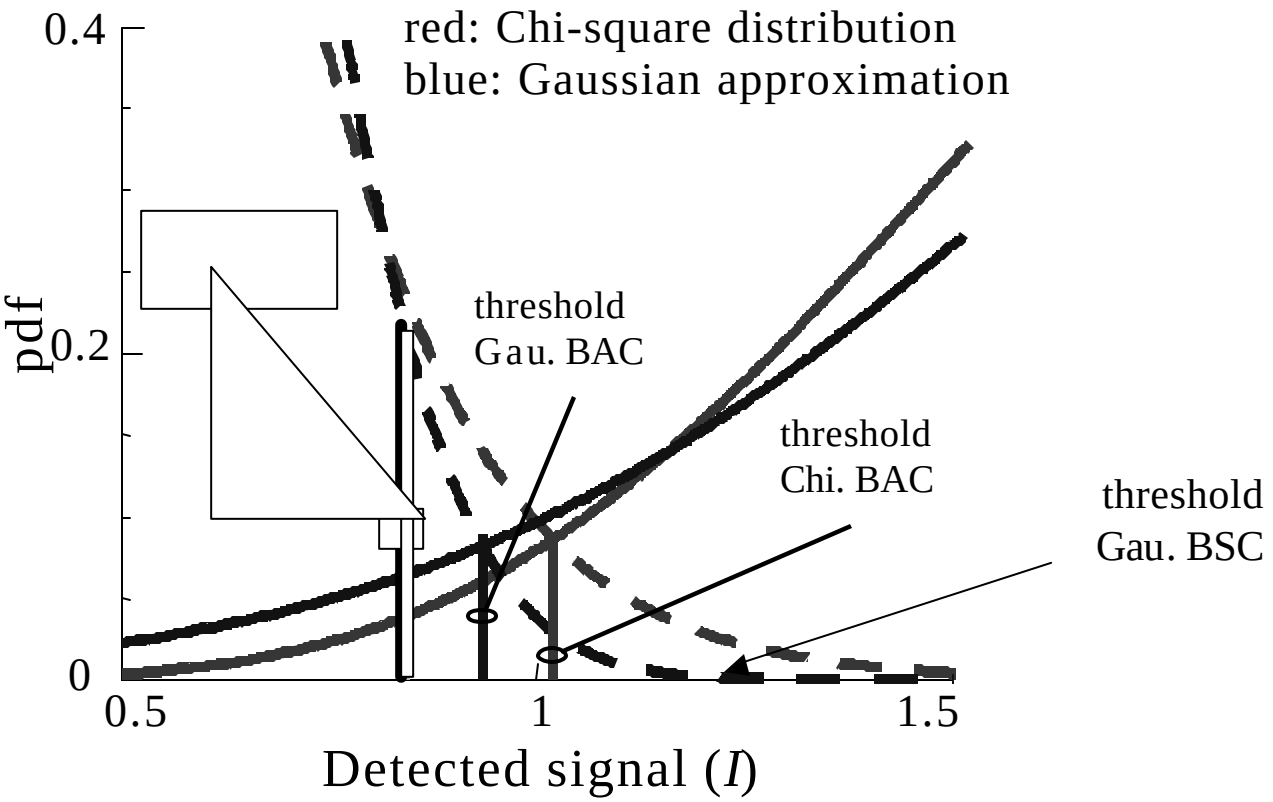
Investigate More Accurate Models for Code/Decision Circuit Studies:

- BAC w/Chi-Square *pdf*s
  - Single threshold
  - Higher channel capacity
  - Requires knowing exact *pdf*s
  - Looking at robust (minimax) decision characterization
- BSC/E
  - Double threshold to generate erasure output plus 0 and 1
  - Higher channel capacity
  - Codes can correct more erasures than errors via $(2e + f) < d_{min}$

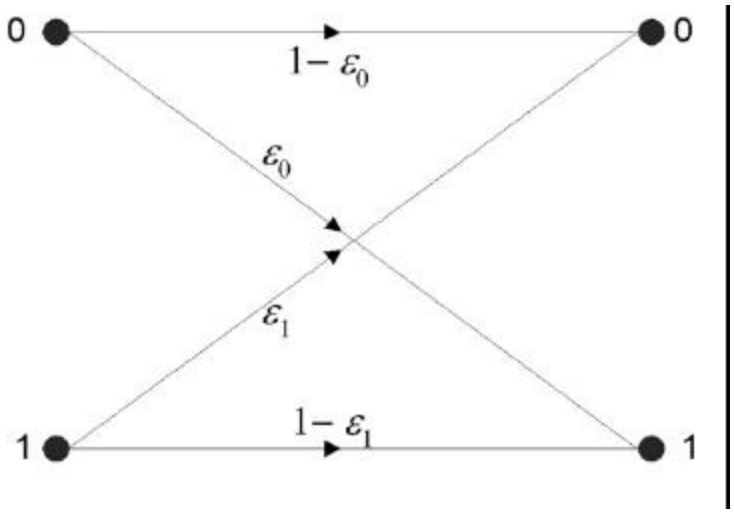
Decision Circuit *pdf*s

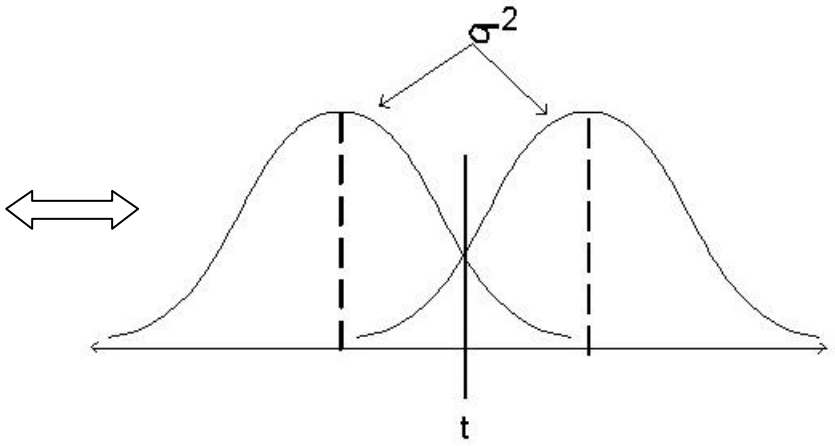


Decision Thresholds for Different Channel Models



One-Threshold Decisioning -- BSC/BAC





$e_0 = e_1 = p \longrightarrow$ BSC

$e_0 \neq e_1 \longrightarrow$ BAC

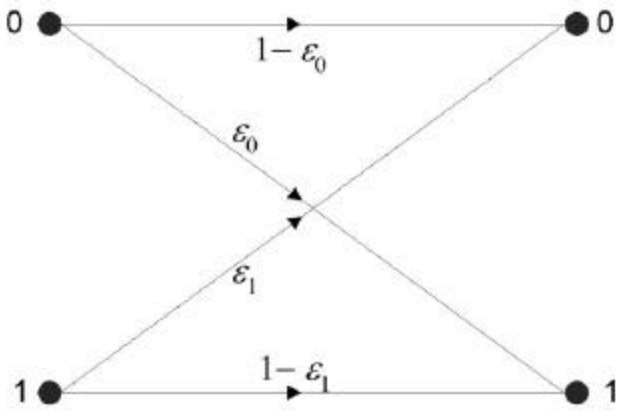
$$P_{CD} = \sum_{i=0}^{t} \binom{n}{i} p^i (1-p)^{n-i}$$

~ Prob. Correct Decoding for BSC

$$P_{ID} = 1 - P_{CD}$$

~ Prob. of Incorrect Decoding for BSC

BSC/BAC Capacity



BSC capacity is $C = 1 - H(p), \qquad p = e_0 = e_1$

BAC capacity is $C = H\left[p_0(1-e_0) + (1-p_0)e_1\right] - p_0 H[e_0] - (1-p_0)H[e_1]$

where $p_0 = 1 - \dfrac{1-(1+k)e_0}{(1-e_0-e_1)(1+k)} \qquad k = \exp\{\dfrac{H(e_1) - H(e_0)}{(\log_2 e)(1-e_0-e_1)}\}$

Chi-Square *pdf* Parameters

$$p_1(I) = \frac{1}{N_0}\left(\frac{I}{E}\right)^{(M-1)/2} exp\left(-\frac{I+E}{N_0}\right) I_{M-1}\left(2\frac{\sqrt{IE}}{N_0}\right)$$

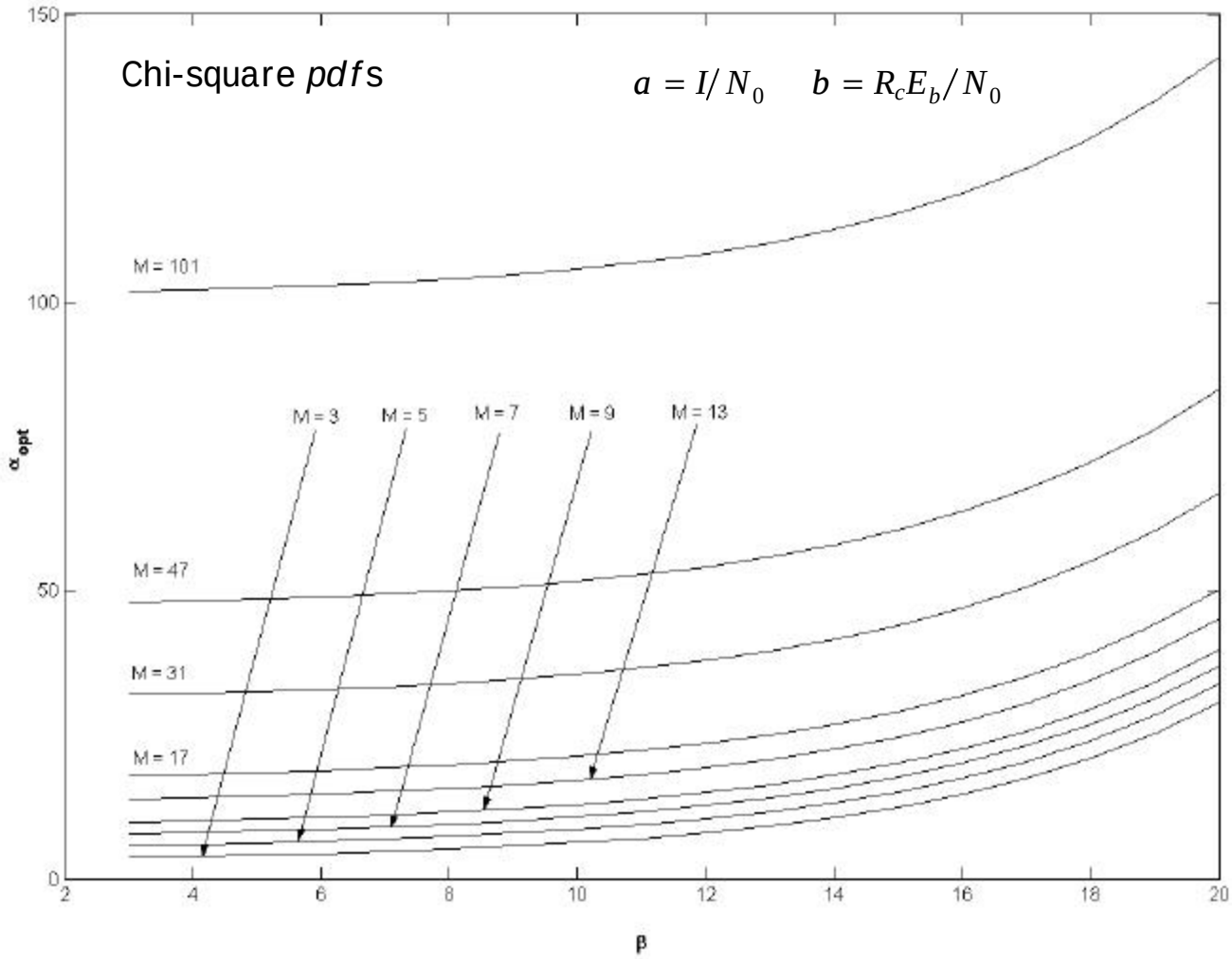
$$p_0(I) = \frac{1}{N_0}\frac{\left(I/N_0\right)^{M-1} exp\left(-I/N_0\right)}{(M-1)!}$$

$$Q = \left(m_1 - m_0\right) / \left(s_1 + s_0\right)$$

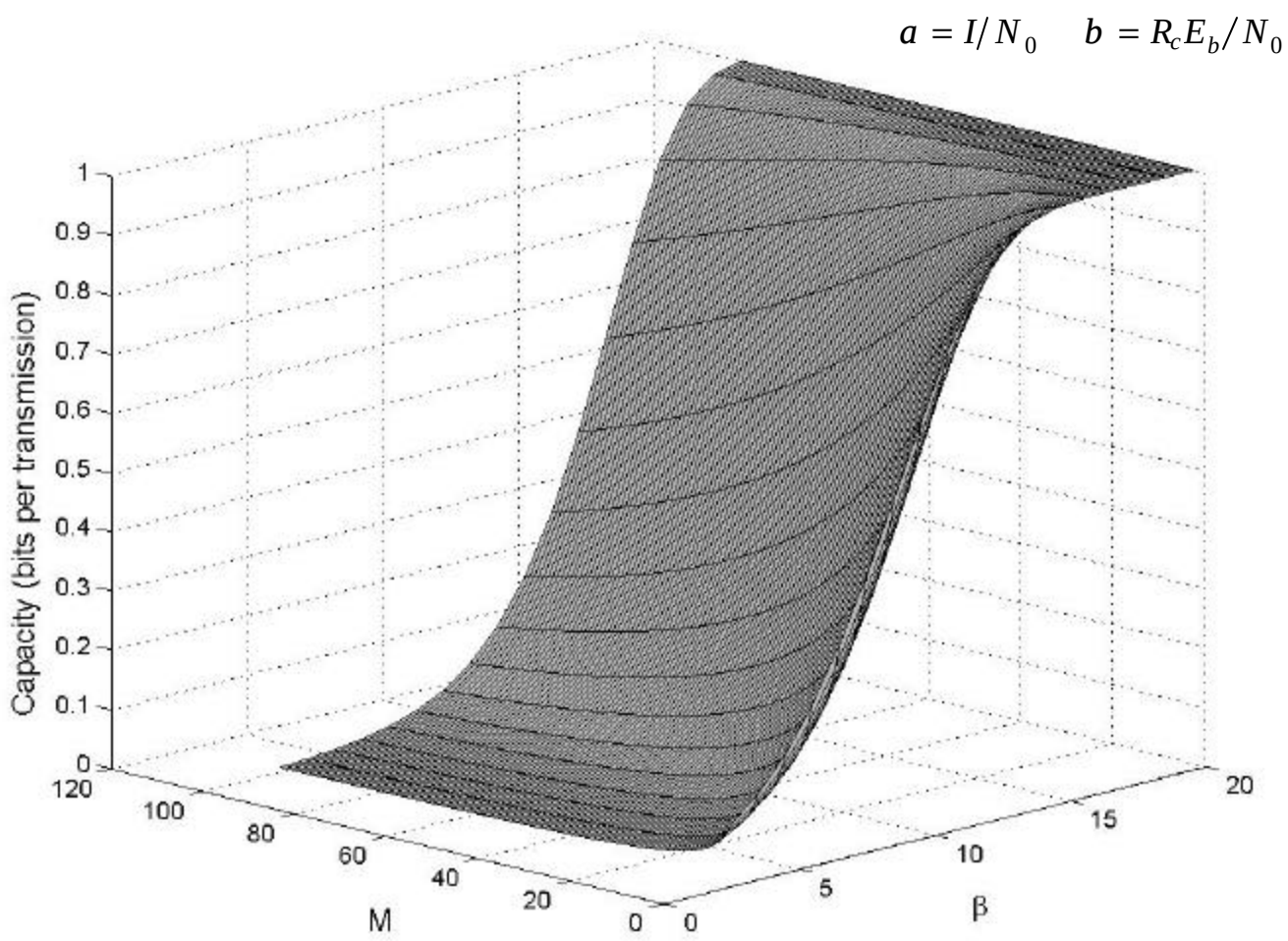
$$s_0 = \sqrt{\frac{B_o}{B_e}} \qquad I_0 = \frac{B_o}{B_e} = M$$

$$s_1 = \sqrt{\frac{B_o}{B_e}} + 2Q \qquad I_1 = 2Q\sqrt{\frac{B_o}{B_e}} + 2Q^2 + \frac{B_o}{B_e}$$

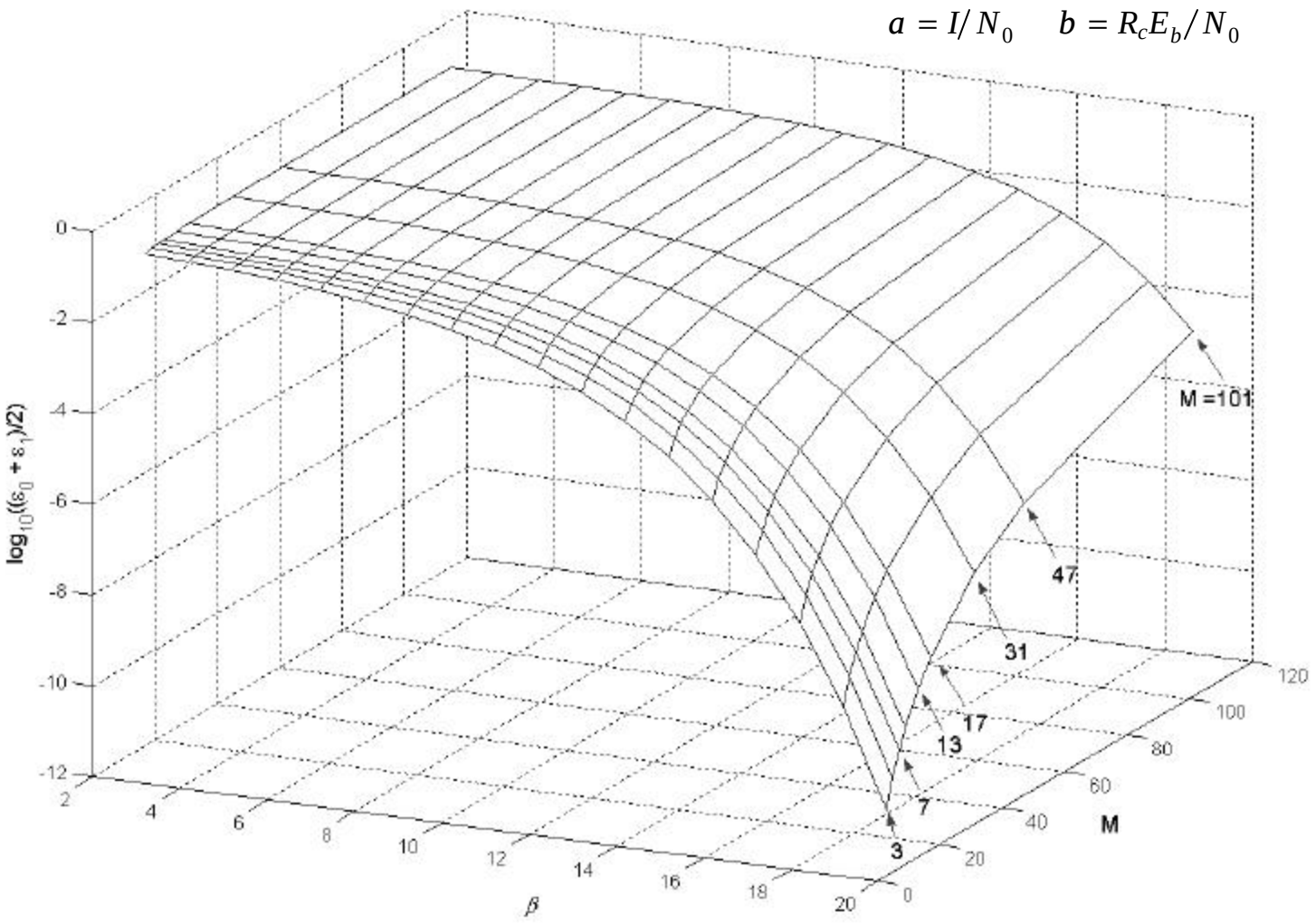
Optimal Decision Thresholds (a_{opt}) vs. b and M



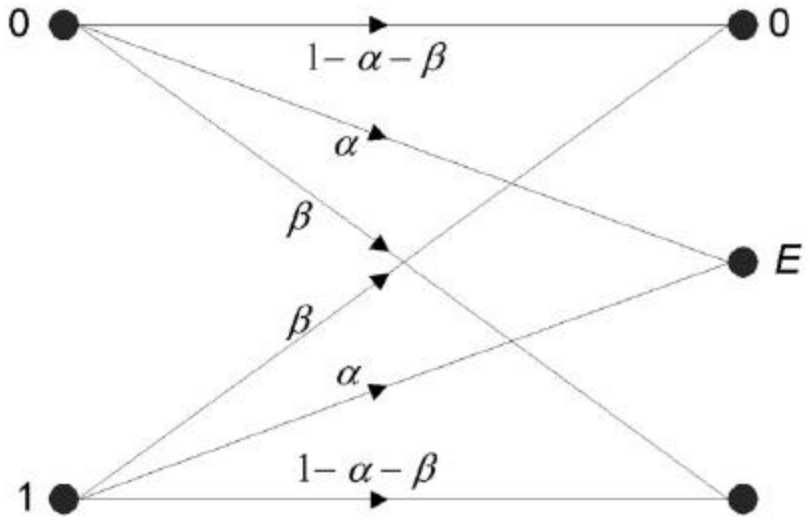
Channel Capacity vs. b and M using a_{opt}

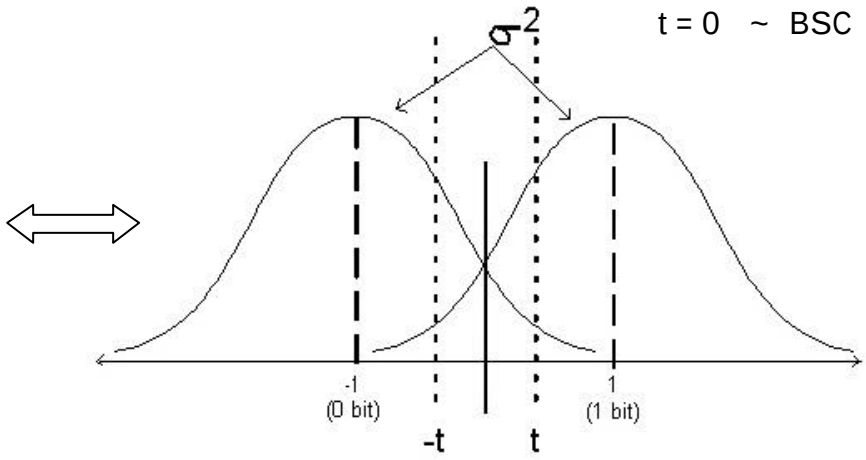


Average P_e as a Function b and M



Two-Threshold Decisioning - BSC/E

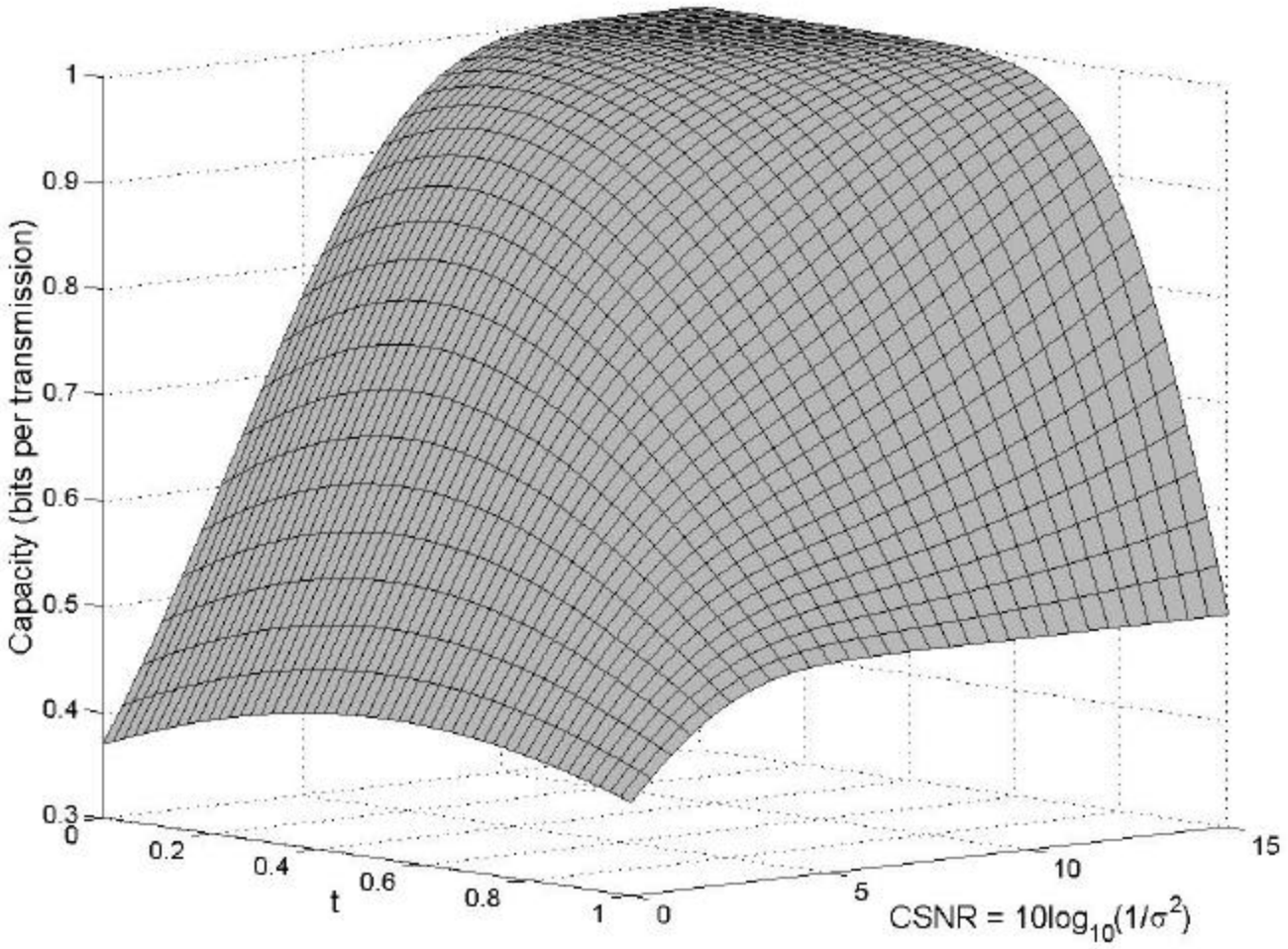




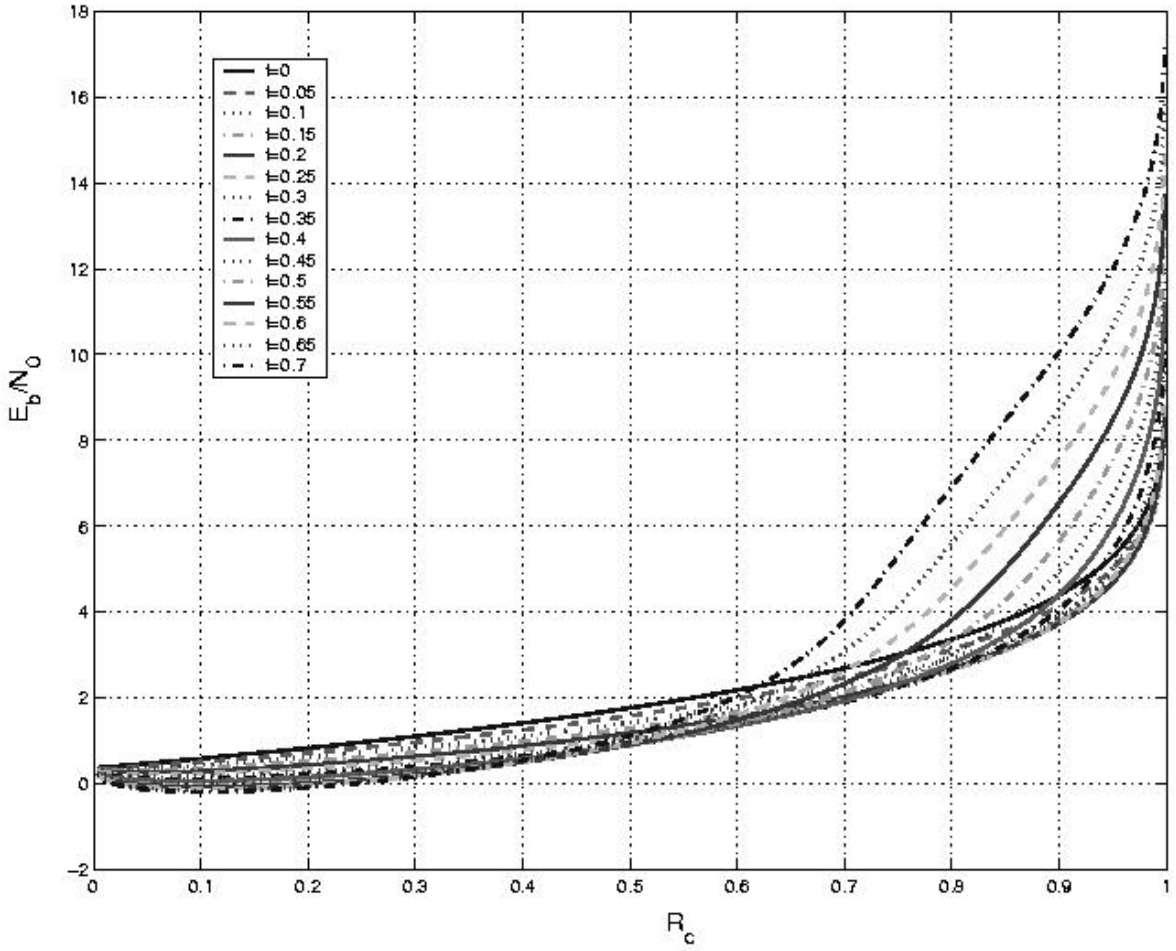
$$C_{BSC/E} = -(1-a)\log_2\left(\frac{1-a}{2}\right) + (1-a-b)\log_2(1-a-b) + b\log_2 b$$

$$a = Q\left(\frac{-t+1}{s}\right) - Q\left(\frac{t+1}{s}\right) \qquad b = Q\left(\frac{t+1}{s}\right) \qquad Q(x) = \frac{1}{\sqrt{2p}}\int_x^\infty e^{-t^2/2}\,dt$$

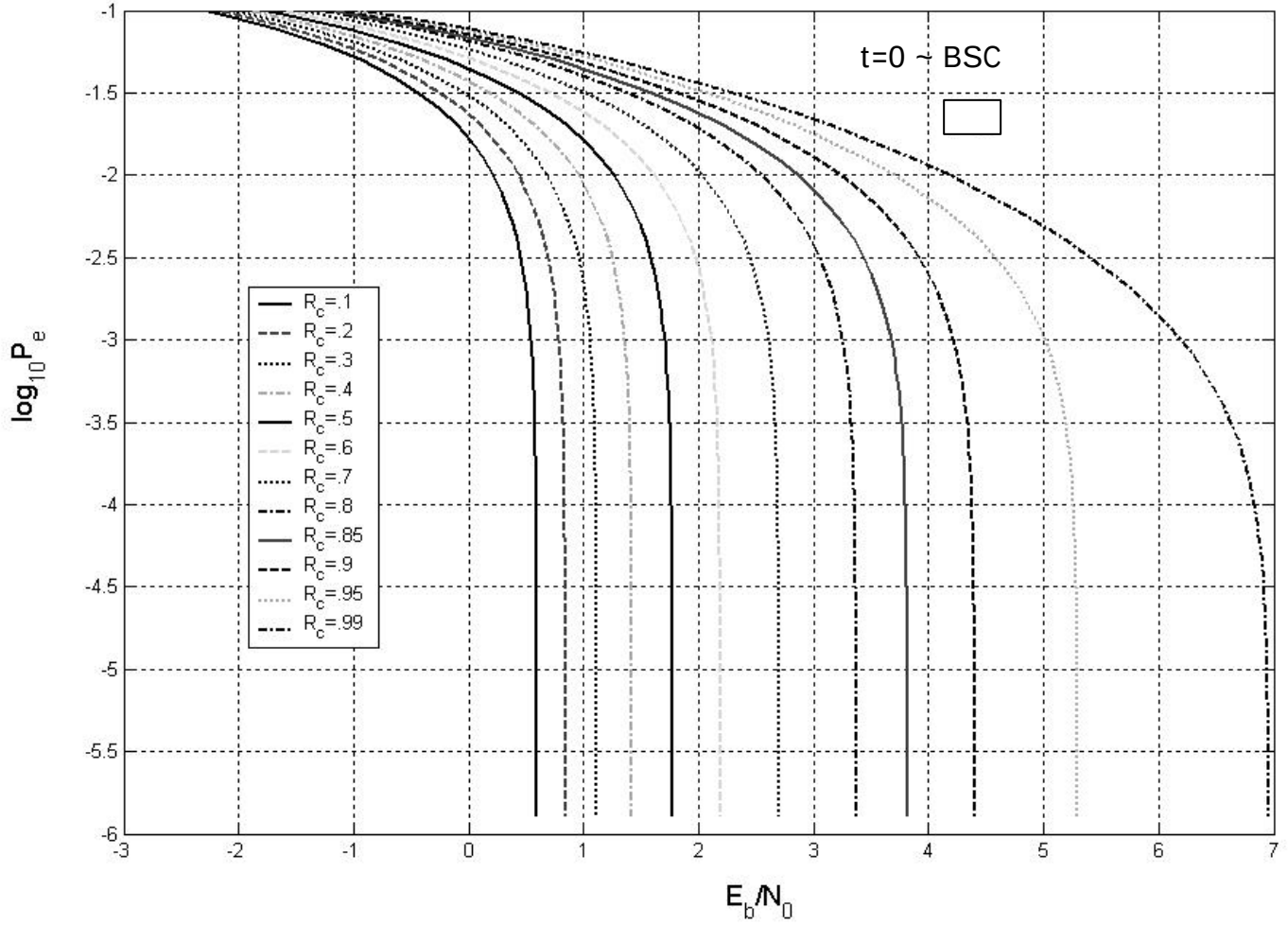
Capacity of BSC/E vs. t and CSNR



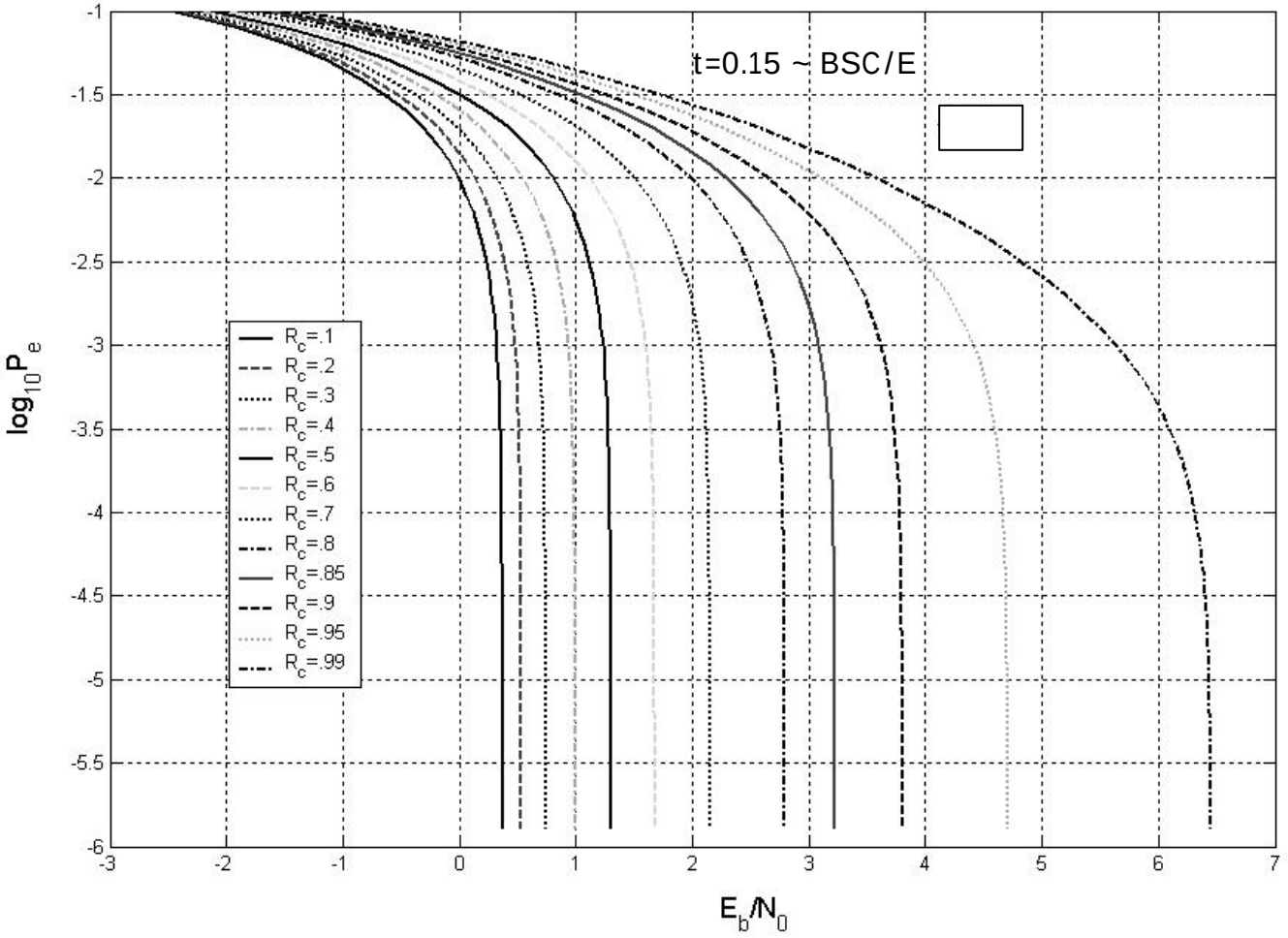
Shannon Limit Curves - BSC/E



Shannon P_e vs. E_b/N_0 Lower Limit Curves - BSC/E



Shannon P_e vs. E_b/N_0 Lower Limit Curves - BSC/E



FEC Decoding for the BSC/E

Hard-decision decoding algorithms for the BSC can be suitably modified to perform decoding for the BSC/E.

Begin with a bounded distance decoder for the BSC and received word w.

1. Replace every location in w that has an erasure with 1 and decode to obtain a resulting codeword c_1.
2. Then replace every location in w that has an erasure with 0 and decode to obtain a resulting codeword c_0.
3. Compute the Hamming distance between the pair w and c_1 and the pair w and c_0.
4. Choose c_1 as the decoder output if its Hamming distance from w is less than that of c_0 from w. Else choose c_0.

Note: An erasure in w contributes equally to both Hamming distances.

FEC Decoding for the BSC/E

The preceding decoder for the BSC/E can correct all patterns of e errors and f erasures as long as $(2e + f) < d_{min}$. Hence it is a bounded distance decoder for the BSC/E.

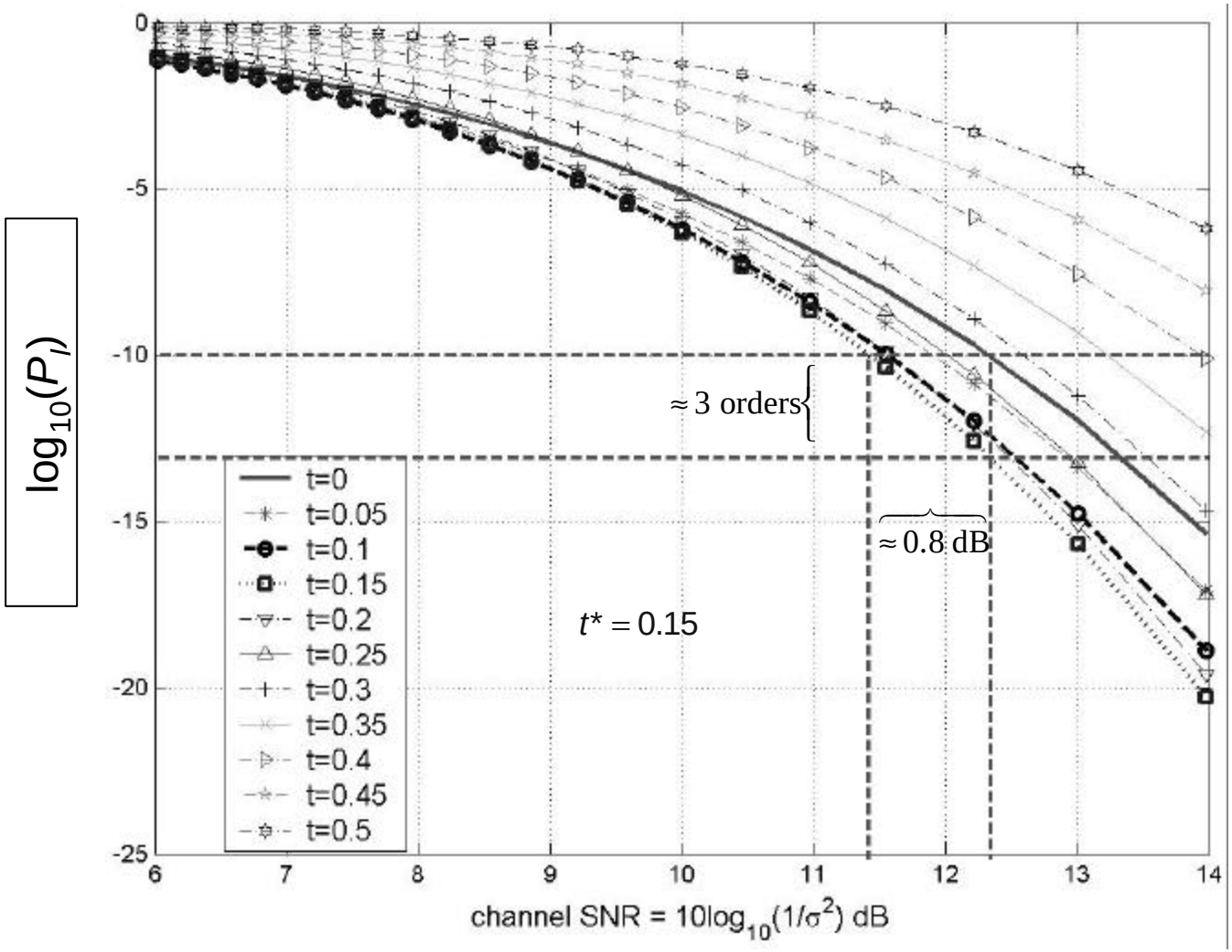
$$P_{CD} = \sum_{e,f \geq 0;(2e+f) < d_{\min}} \binom{n}{f}\binom{n-f}{e} a^f b^e (1-a-b)^{n-f-e}$$

~ Prob. of Correct Decoding

$$P_I = 1 - P_{CD}$$

~ Prob. of Incorrect Decoding

$P_l^{(t)}$ vs. *CSNR* Plots



$n = 49$

$d_{min} = 6$

RCD SPC

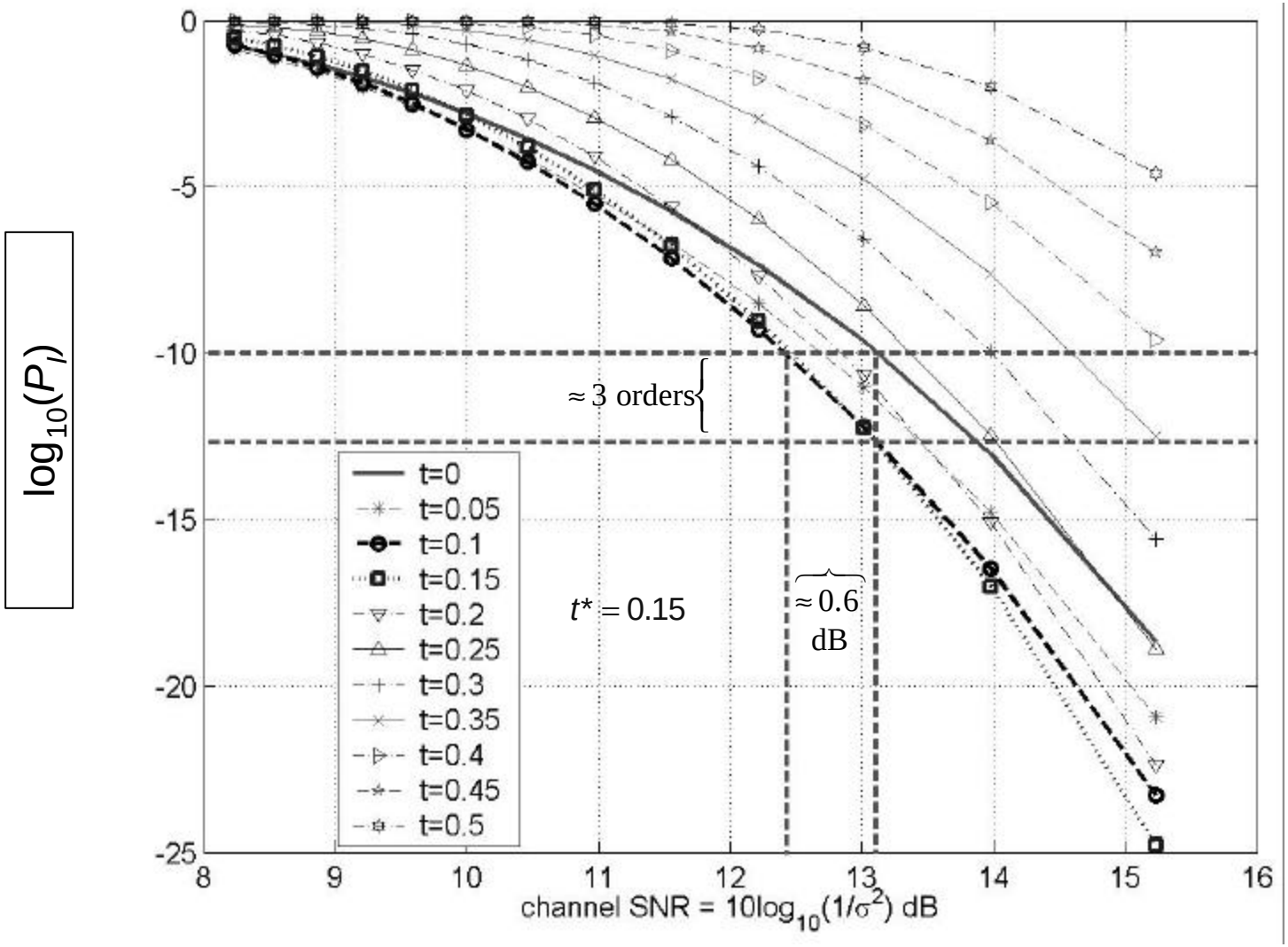
For $R_c = 0.6122$

Shannon Limit for BSC (CSNR) = 3.12 dB

and

Shannon Limit for BSC/E (CSNR) with $t^* = 0.15$ = 2.61 dB

$P_I^{(t)}$ vs. *CSNR* Plots



$n = 289$

$d_{min} = 6$

RCD SPC

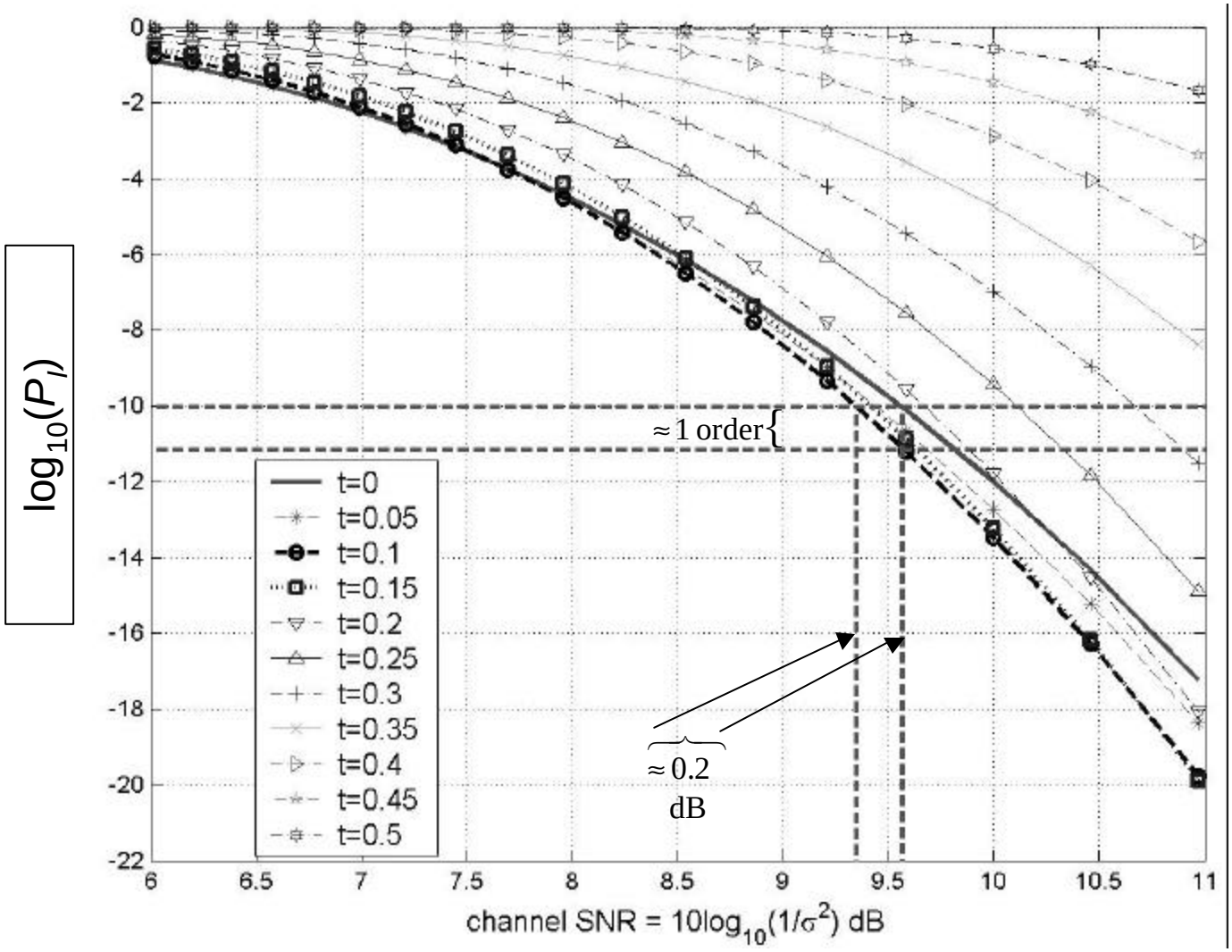
For $R_c = 0.8304$

Shannon Limit for BSC (CSNR) = 5.83 dB

and

Shannon Limit for BSC/E (CSNR) with $t^* = 015$ = 5.25 dB

$P_l^{(t)}$ vs. *CSNR* Plots



$n = 255$

$d_{min} = 17$

EG

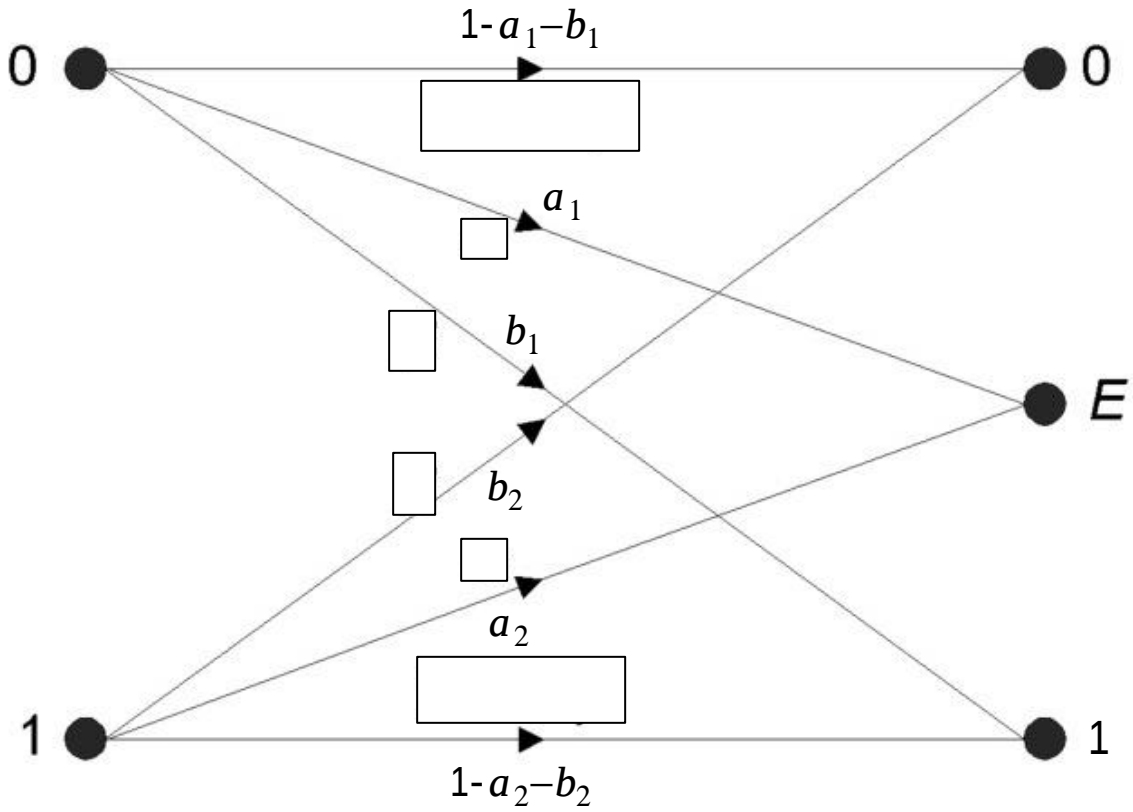
For $R_c = 0.6863$

Shannon Limit for BSC (CSNR) = 4.00 dB

and

Shannon Limit for BSC/E (CSNR) with $t^* = 0.1$ = 3.60 dB

BAC/AE Channel Model



Related Conclusions

- Using two-thresholds (BSC/E) provides coding and capacity gains over the one-threshold (BSC).
- Gains achieved by only doubling decoding and decisioning complexity.
- Improvements in employing a BSC/E channel model:
  - Decrease with increasing n and d_{min}
  - Decrease with increasing P_I

Performance (Ideal) Assessment via Bounds and Simulations

- Union Bound on BER/WER vs. E_b/N_o requires Weight Enumerator Function (WEF) for Code

$$W(z) = \sum_{d=0}^{n} A_d z^d, \qquad \{A_d\} \sim \text{WEF coefficients}$$

- Simulations for BER/WER vs. E_b/N_o require major computing power/time, or modified importance sampling (IS)

  ~ Multicanonical Monte Carlo technique under investigation

Error Correction Capability wrt d_{min} (BSC)

Weight distribution

Bounded distanced decoding (BDD)

$$P_E = \sum_{d=d_{\min}}^{n} A_d \sum_{k=0}^{t} P_k^d$$

~ Prob. Decoder Error

$$P_k^d = \sum_{m=0}^{k} \left(\frac{d}{k-m} \right) \left(\frac{n-d}{m} \right) p^{d-k+2m} (1-p)^{n-d+k-2m}$$

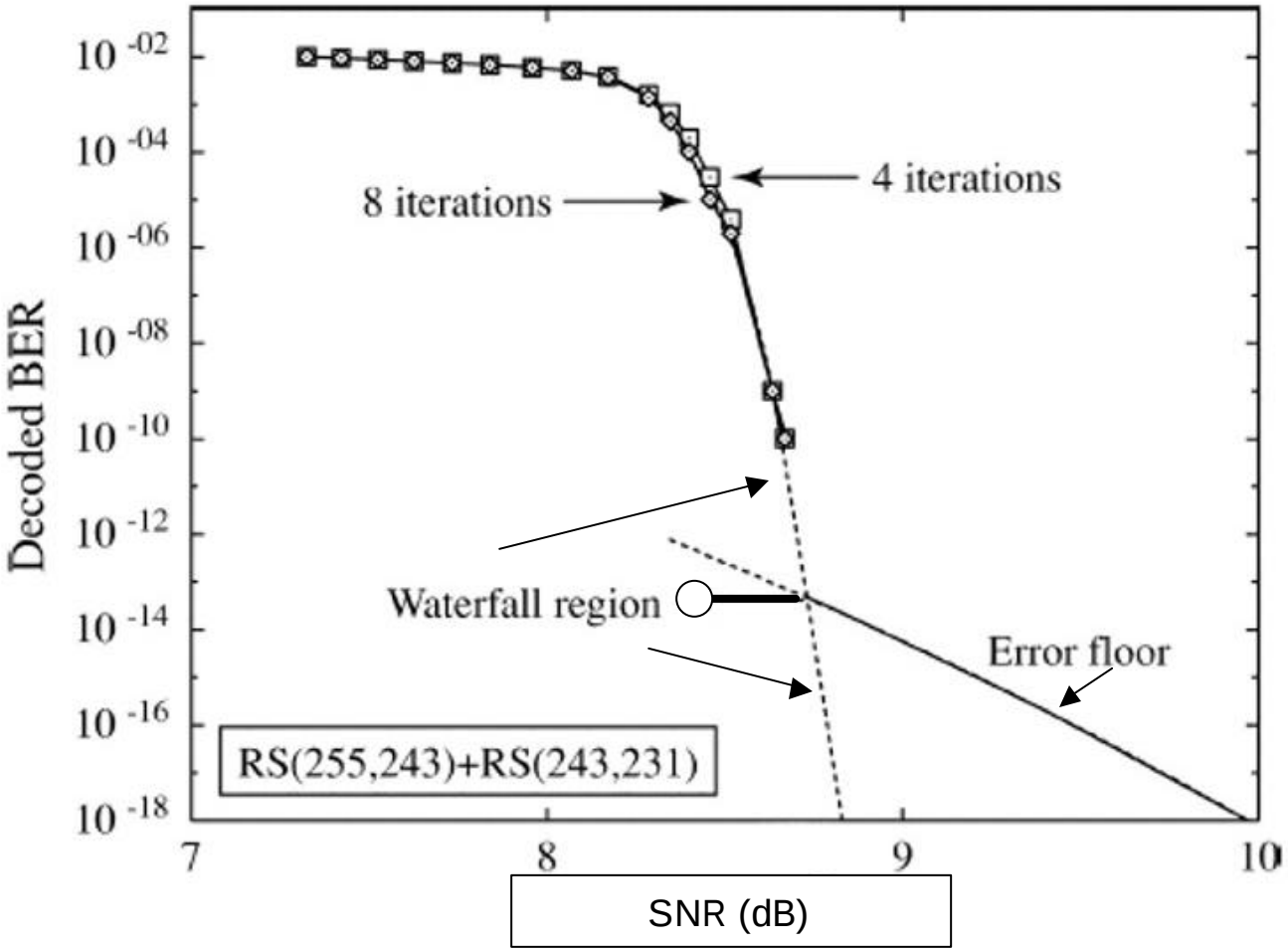
$$P_{CD} = \sum_{i=0}^{t} \binom{n}{i} p^i (1-p)^{n-i}$$

~ Prob. Correct Decoding

$$P_F = 1 - P_{CD} - P_E$$

~ Prob. Failure

Water-Fall and Error-Floor Behavior



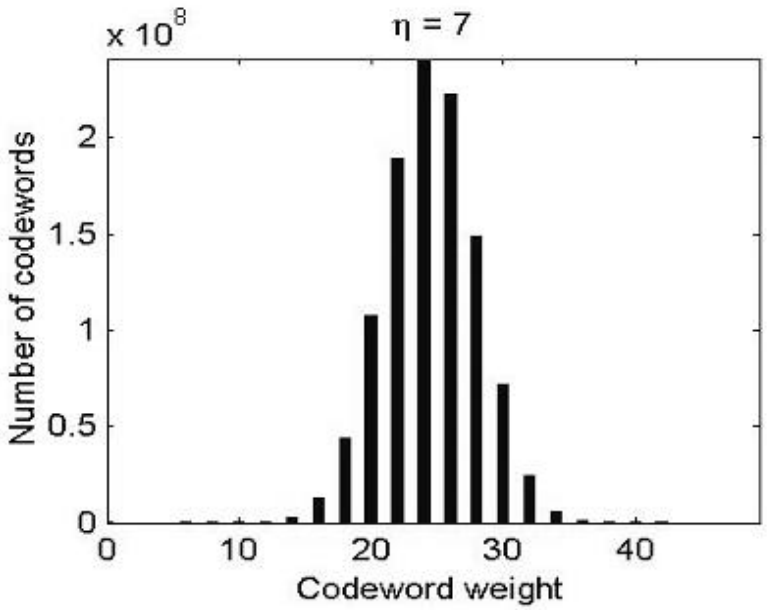
RCD-LDPC Code WEF

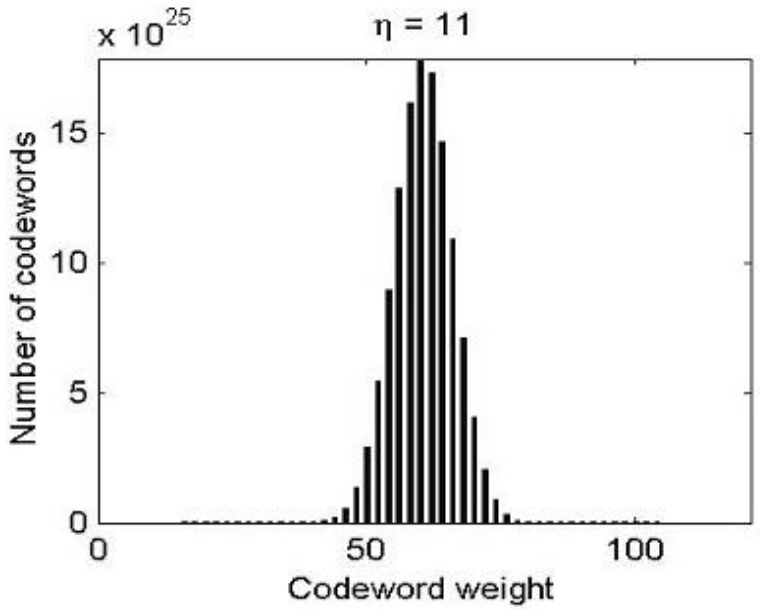
The RCD code WEF is given by

$$W(z) = 2^{-(3h-2)}(1+z)^{h^2} \cdot \sum_{a=0}^{h} \sum_{b=0}^{h-1} \sum_{c=0}^{h-1} h_a h_b \frac{h-b}{h} \frac{h-c}{h} \sum_{m=1}^{K_{a,b}} p_m \left(\frac{1-z}{1+z}\right)^w \sum_{n=1}^{N_{m,c}} \prod_{l=1}^{L_m} \binom{h_{l,m}}{\Delta_{l,n}} \left(\frac{1-z}{1+z}\right)^{-2\Delta_{l,n} I_{l,m}}$$

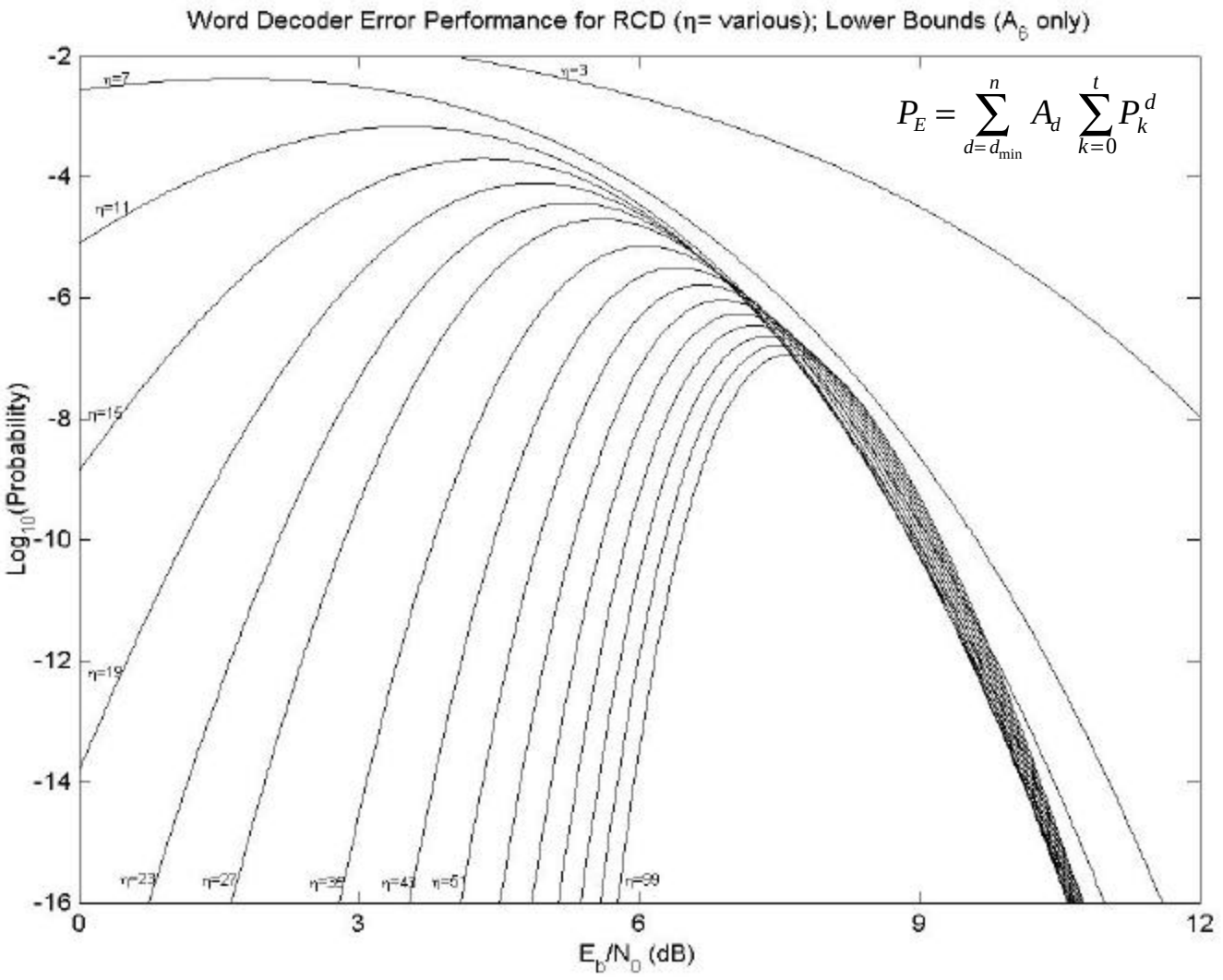
RCD-LDPC Code WEF Plots

WEF plots for RCD codes of n = 49 and 121





$d_{\min}$ (= d_6) Component of RCD WER



Related Conclusions

- Solution for WEF for a class of LDPC codes obtained
- Results show the RCD-LDPC codes are weakly-random-like codes with WEF approximately Binomial for moderate code lengths *n*
- Technique likely extendable to related classes of LDPC codes
- Important for WER/BER vs. SNR performance assessment

Performance (Non-Ideal) Assessment via Implementation Issues

- Effect of Mismatched/Incorrect Decision Circuit Statistics on SPA
  - Incorrect estimate of initial statistics
  - Time-varying statistics
- Effect of Logic Circuit Errors on Majority-Logic Decoding

  e.g., optical logic devices have appreciable error rates

SPA Sensitivity to Channel Noise Assumptions

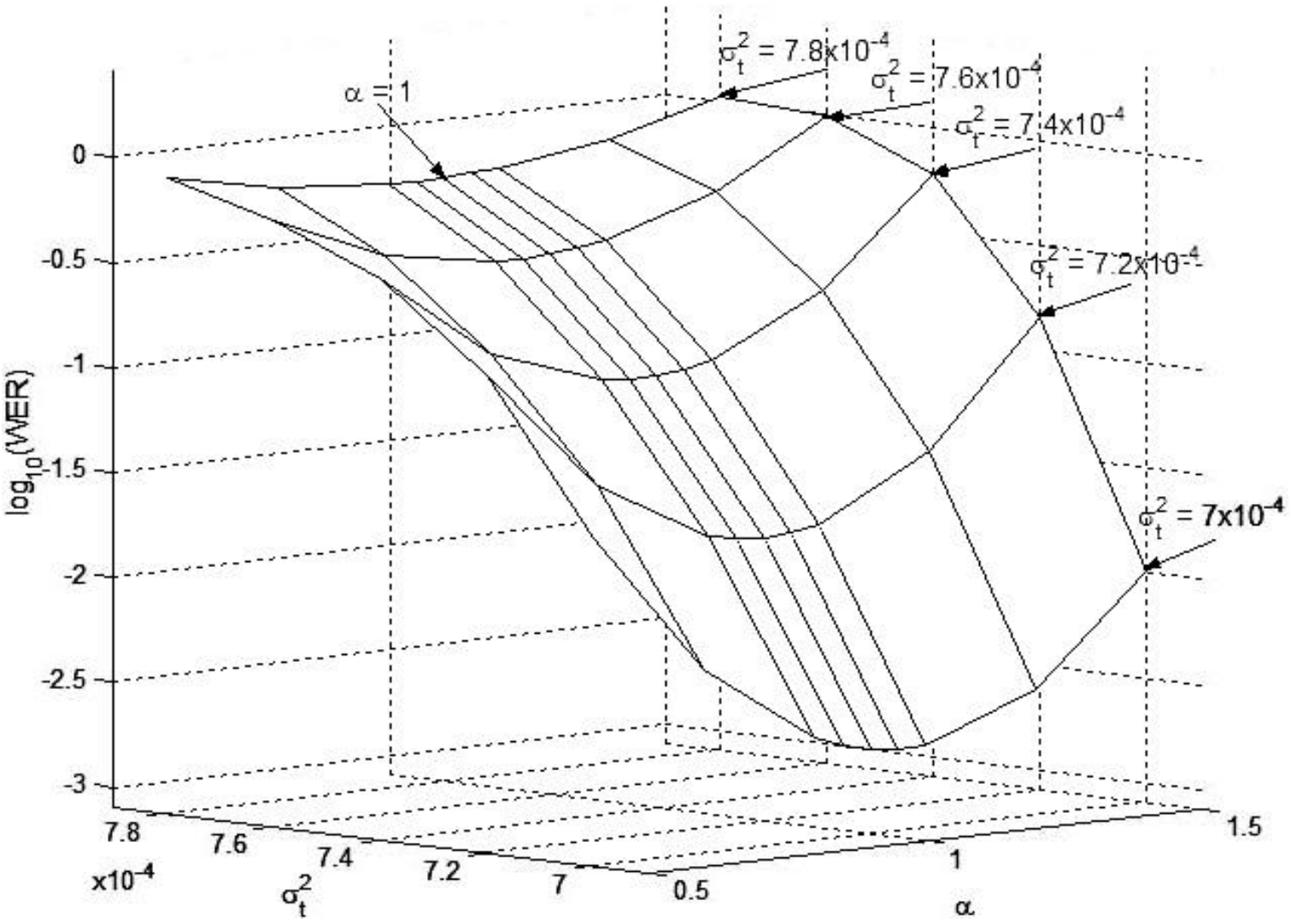
- We define $a = \frac{s_a^2}{s_t^2}$ where,

  s_a^2 = assumed noise variance for APP computation

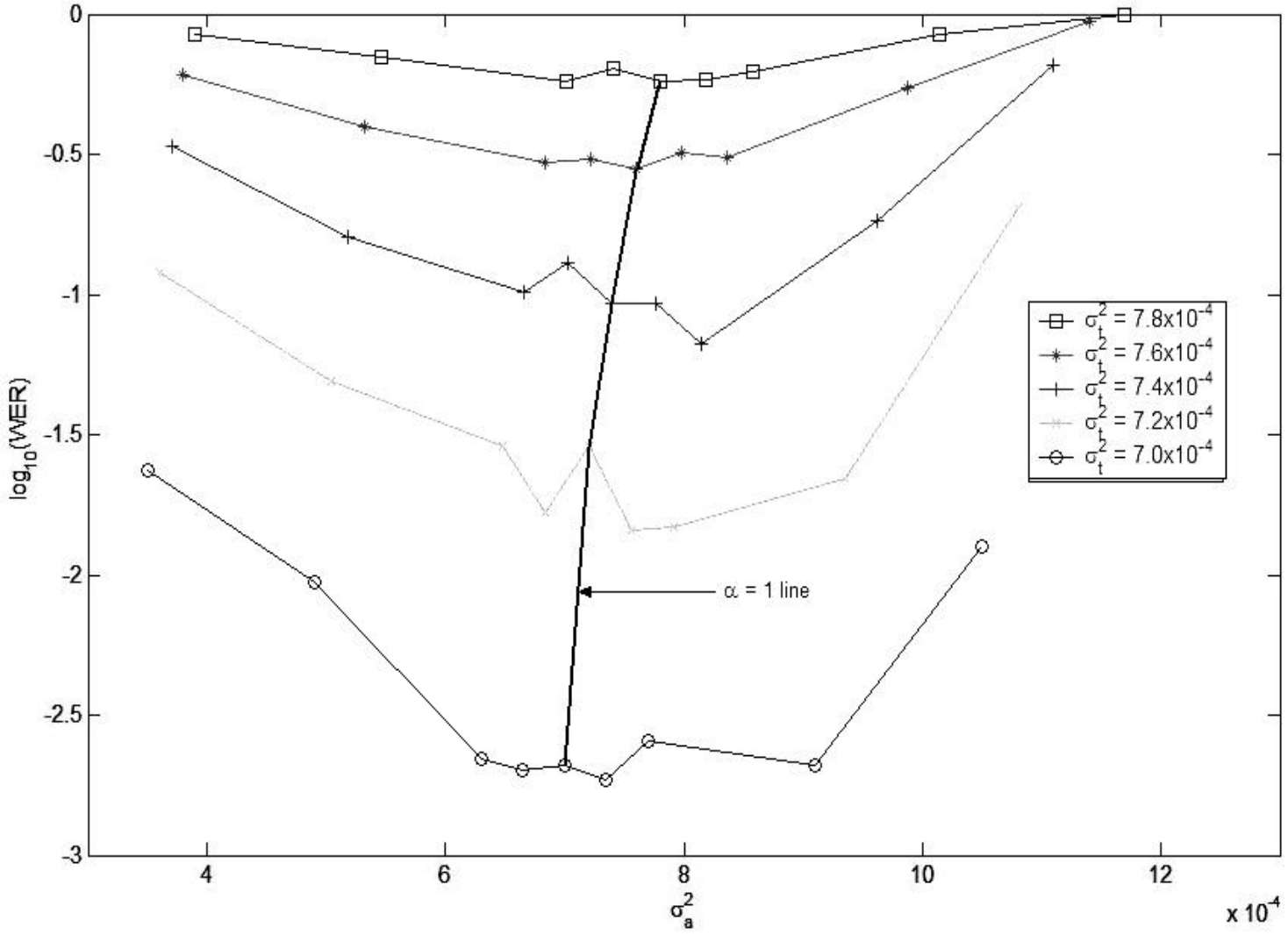
  s_t^2 = true noise variance on channel

- s_a^2 is set during initialization

Surface Plot of WER vs. a and $s_t^?$



2D Plot of WER vs. s_a^2 for Given s_t^2



Related Conclusions

- Performance of SPA is sensitive to changes in noise variance s^2.
- WER and BER were observed to be "asymmetrical" about $a = 1$ when s^2 is fixed.
- Results indicate the range of inaccuracy allowable in estimating s^2 to achieve a given performance tolerance.
- There is a broad minimum for WER wrt a where WER remains within twice that at $a = 1$ when s^2 is fixed.
- Increase in WER is more rapid beyond this range.
- It may be advantageous to assume a s^2 that is 1.05 - 1.1 times that of the true value during initialization -- yields a more "symmetrical" performance wrt noise variations.

Logic Circuit Errors: Motivation

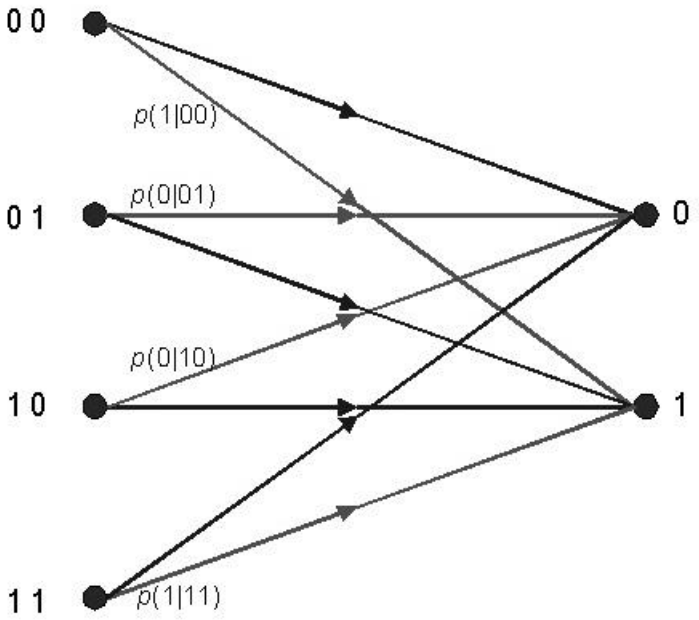
- Traditionally, logic devices such as OR, AND, XOR-gates have been assumed to perform perfectly without introducing any errors at the output.
- However, for CMOS devices, as they approach the fundamental physical limits, or for logic devices implemented in the optical domain, this assumption may no longer be true.
- More stringent requirements on the probability of error that can be tolerated on communication channels may also render this assumption tenuous, e.g., optical channels demand a BER of ~10^{-15}.

Error Model for Simple Logic Devices

- Probability transition matrices can model errors introduced by logic devices.
- 2-inp XOR gate
  - 4 i/p states
  - 2 o/p states

$$\begin{array}{c} \\ 0 \\ 1 \end{array}\begin{array}{c} \begin{array}{cccc} 0\,0 & 0\,1 & 1\,0 & 1\,1 \end{array} \\ \left[\begin{array}{c|c|c|c} 1-p(1|00) & p(1|01) & p(1|10) & 1-p(1|11) \\ p(1|00) & 1-p(1|01) & 1-p(1|10) & p(1|11) \end{array}\right] \end{array}$$

Ip 1	Ip 2	Op
0	0	0
0	1	1
1	0	1
1	1	0



Analysis of Error Introduced by a Logic Circuit System

- Simplest technique: Find probability of correct output (P_c) for each logic device from its transition matrix. Probability of error at the output of the logic circuit, (P_E) is given as

$$P_E = 1 - \prod_{\text{All logic devices}} P_C$$

- For a more accurate analysis, one has to determine the overall transition matrix that relates the output of the logic circuit to its inputs.
  - Logic circuit specific
  - May not be easy
  - Need to exploit whatever independence exists among input variables

Related Conclusions

- Logic gates with internal errors, particularly optical logic gates, can affect the error performance of MLG decoders
- Similar effects expected for other logic circuit systems
- An analysis method is under development, based on a probability transition matrix approach.

Related Publications

1. "On RCD SPC Codes as LDPC Codes Based on Arrays and Their Equivalence to Some Codes Constructed from Euclidean Geometries and BIBDs", UMBC Technical Report No.: CSPL TR: 2002-1, June 2002
2. "On the Sensitivity of the SPA for LDPC Codes …… to Variations in Channel Noise", *2003 Conf Inform. Sci. and Sys.* (*CISS2003*), The Johns Hopkins University, 12-14 Mar. 2003.
3. "On Minimum Probability of Error Decision Thresholds for FEC Codes on the BSC/E …….", *CISS2003*, 12-14 Mar. 2003.
4. "On the Weight Enumerator Function for a Class of Regular LDPC Codes", *CISS2003*, 12-14 Mar. 2003.
5. "On FEC Code Performance Improvement Comparisons between the BSC and the BSC/E under Bounded Distance Decoding", *2003 Canadian Workshop on Inform. Thy*, Waterloo, Ontario, 18-21 May 2003.
6. "The RCD Array Code is a Weakly Random-Like Code", to appear *3rd Int'l. Symp. on Turbo Codes and Related Topics*, Brest, France, 1-5 Sept. 2003.
7. "A Performance Surface Characterizing Sensitivity to Incorrect Channel Noise Statistics for SPA Decoding of LDPC Codes ……", to appear *3rd Int'l. Symp. on Turbo Codes and Related Topics*, Brest, France, 1-5 Sept. 2003.

Related Publications

8. W. Martin, “The WEF for a Class of Regular LDPC Codes: The RCD Array Code”, PhD Dissertation, 2003, CSEE Dept., UMBC, Catonsville, MD 21250